



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/544,822	04/06/2000	Tongbi Jiang	4241US	9308
7590	06/14/2005		EXAMINER	
James R Duzan Trask Britt & Rossa P O Box 2550 Salt Lake City, UT 84110				GRAYBILL, DAVID E
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/544,822	JIANG, TONGBI	
	<b>Examiner</b> David E. Graybill	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 21 March 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-5,7-32 and 58-64 is/are pending in the application.
- 4a) Of the above claim(s) 33-57 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-5,7-32 and 58-64 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 64 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yamada (5959363).

At column 53, line 65 to column 56, line 11; and column 59, lines 34-44, Yamada discloses a method for applying a material between a semiconductor device 201 having a surface and a substrate 202 having a surface, said semiconductor device mounted on said substrate, said method comprising: applying a essentially uniform liquid (alcoholate) wetting agent layer 208 inherently having a thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material 206 between the substrate and the semiconductor device separately from said liquid wetting

agent layer, such that said flowable material contacts said wetting agent layer.

To further clarify, the layer inherently is at least a monolayer thick, and, when the total thickness is greater than a monolayer, the layer inherently has a thickness of about a monolayer at least intermediate the total thickness of the layer.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (5959363).

Yamada is applied as it is applied supra.

However, Yamada does not appear to explicitly disclose the particular claimed layer thickness.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular thickness because applicant has not disclosed that, in view of the applied prior art, this layer dimension is for any additional purpose, and it appears *prima facie* that

the process would possess utility using another thickness. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 1-5, 7-12, 15, 22 and 58-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dery (6074895) and Plueddemann (4231910).

At column 1, lines 51-62; column 2, line 52 to column 5, line 11; column 5, lines 51-59; and column 6, lines 13-54, Dery discloses, Dery discloses the following:

A method for applying a material between a semiconductor device 110 having a surface 111 and a substrate 120 having a surface 124, said method comprising: applying a wetting agent layer ("treated" surface) to one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material 140 between the substrate and the semiconductor device, such that said flowable material contacts said wetting

agent layer; wherein said semiconductor device is attached to said substrate; wherein said applying said wetting agent layer comprises any one of a dispensing (dispensing plasma) method, a brushing method "an abrasive object 128 (such as a polishing cloth) is shown being moved back and forth," and a spraying method; wherein said wetting agent layer comprises at least one layer; wherein said wetting agent layer comprises a plurality of layers; and wherein said applying a wetting agent layer comprises providing a material that to the surface of one of said surface of said semiconductor device and said surface of said substrate for the application of an underfill material 140.

A method for applying a material between a semiconductor device and a substrate, said method comprising: providing a semiconductor device having an active surface 111, another surface, a first end, a second end, a first lateral side, and a second lateral side "all four sides," said first end, said second end, said first lateral side, and said second lateral side forming at least a portion of a periphery of said semiconductor device; providing a substrate having an upper surface 124, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; and applying a flowable underfill

material between said semiconductor device and said substrate, such that said flowable material contacts said applied wetting agent layer; wherein said flowable material is applied substantially adjacent to at least one end of said semiconductor device; wherein said flowable material substantially fills a gap between said semiconductor device and said substrate; wherein said flowable material is provided substantially adjacent to said at least a portion of the periphery of said semiconductor device to fill a gap between said substrate and said semiconductor device; and wherein said applying said flowable material comprises: providing said flowable material substantially adjacent said first end "one or more edges" of said semiconductor device for filling between said substrate and said semiconductor device by one or more forces acting upon said flowable material.

A method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device having an active surface; providing a substrate having an upper surface; applying a wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device, such that said

flowable underfill material contacts said applied wetting agent layer; wherein applying said wetting agent layer comprises any one of a dispensing method, a brushing method, and a spraying method; and wherein said wetting agent layer comprises at least one layer.

A method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device having an active surface, a first end, a second end, a first lateral side end and a second lateral side end; providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a material layer ("treated" surface) to one of a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate; connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable underfill material between said semiconductor device and said substrate, such that said flowable underfill material contacts said applied material layer.

However, Dery does not appear to explicitly disclose applying a liquid wetting agent layer; the flowable material contacts said liquid wetting agent layer; wherein said liquid wetting agent layer includes a layer of silane-

based material; wherein said liquid wetting agent layer comprises one of glycidoxypropyltrimethoxysilane and ethyltrimethoxysilane.

Nonetheless, at column 1, lines 5-8, 21-23 and 55-63; column 2, lines 5-49; column 3, lines 22-54; column 3, line 65 to column 4, line 10; column 4, lines 24-27 and 58-62; column 6, lines 11-19, 37-44 and 57-65; and column 7, line 4 to column 8, line 5, Plueddemann discloses applying a liquid wetting agent layer; a flowable material contacts said liquid wetting agent layer; wherein said liquid wetting agent layer includes a layer of silane-based material; wherein said liquid wetting agent layer comprises one of glycidoxypropyltrimethoxysilane and ethyltrimethoxysilane. In addition, it would have been obvious to combine the processes of Plueddemann and Dery, for example, by substituting or combining the wetting agent layer of Plueddemann for or with the wetting agent layers of Dery because both Plueddemann and Dery are drawn to improving adhesion of a plastic and the process of Plueddemann would improve the adhesion of the plastic of Dery.

In addition, it has been held that it is obvious to combine two processes for the same purpose. *In re Novak* 16 USPQ2d 2043. Similarly, "It is *prima facie* obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose . . . [T]he idea of

combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted) (Claims to a process of preparing a spray - dried detergent by mixing together two conventional spray - dried detergents were held to be prima facie obvious.). See also, In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) (Claims directed to a method and material for treating cast iron using a mixture comprising calcium carbide and magnesium oxide were held unpatentable over prior art disclosures that the aforementioned components individually promote the formation of a nodular structure in cast iron.); and Ex parte Quadranti 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992) (Mixture of two known herbicides held prima facie obvious).

Incidentally, when the wetting agent layers of Dery and Plueddemann are used in conjunction, the liquid wetting agent layer comprises a plurality of layers.

Claims 13, 14, 16-21 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dery and Plueddemann as applied to claims 1-5, 7-12, 15, 22 and 58-63 supra, and further in combination with Akram (5766982).

Dery and Plueddemann do not appear to explicitly disclose the following:

The method wherein said substrate includes an aperture extending through said substrate; wherein said aperture is located adjacent to said another surface of said semiconductor device, further comprising: elevating at least said first side wall of said substrate and said first end of said semiconductor device; wherein said elevating said first side wall of said substrate comprises placing said substrate on a support structure and elevating at least one portion of said support structure, further comprising: providing a dam on the substrate adjacent to at least one of said first end, said second end, said first lateral side and said second lateral side of said semiconductor device; wherein said dam extends to substantially between said semiconductor device and said substrate, further comprising: vibrating one of said semiconductor device and said substrate; wherein said vibrating one of said semiconductor device and said substrate comprises placing said substrate on a support structure and vibrating said support structure; wherein said substrate includes at least one aperture extending through said substrate and substantially located adjacent to said another surface of said semiconductor device; wherein said flowable material is provided through said at least one aperture of said substrate substantially filling a gap.

between said substrate and said semiconductor device; wherein said substrate includes at least one aperture extending therethrough and substantially located adjacent to said another surface of said semiconductor device; wherein said flowable material is provided from below said substrate; and wherein said flowable material is provided through said at least one aperture contacting at least a portion of said another surface of said semiconductor device.

Nevertheless, at column 4, line 36 to column 7, line 17, Akram discloses a process wherein a substrate 10 includes an aperture extending through a substrate, an aperture 60 is located adjacent (nearby) to another surface of a semiconductor device 12; elevating at least a first side wall of the substrate and a first end of the semiconductor device; wherein elevating a first side wall of the substrate comprises placing the substrate on a support structure 44 and elevating at least one portion of a support structure; providing a dam 40 on the substrate adjacent to at least one of a first end, a second end, a first lateral side and a second lateral side of a semiconductor device; wherein a dam extends to substantially between a semiconductor device and a substrate; vibrating 48 one of a semiconductor device and a substrate; wherein vibrating one of a semiconductor device and a substrate comprises placing a substrate on a support structure and

vibrating a support structure; wherein a flowable material 28 is provided through at least one aperture of a substrate substantially filling a gap 26 between a substrate and a semiconductor device; and wherein a flowable material is provided through a at least one aperture contacting (at least indirectly physically and thermally contacting) at least a portion of another surface of a semiconductor device.

Moreover, it would have been obvious to combine the process of Akram with the process of Dery and Plueddemann because it would facilitate applying the flowable material 140 between the substrate and the semiconductor device.

Also, in the combination, Dery discloses the following:

The method wherein applying a flowable material comprises: providing a flowable material substantially adjacent to a first end of a semiconductor device for filling a gap between a substrate and a semiconductor device; wherein said applying said flowable material comprises: providing said flowable material substantially adjacent to said first end and one of said first lateral side and said second lateral side of said semiconductor device for filling a gap between said substrate and said semiconductor device; and wherein a flowable material is provided from below a substrate.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dery and Plueddemann as applied to claim 10 supra, and further in combination with Banerji (5203076).

Dery and Plueddemann do not appear to explicitly disclose the following:

The method wherein said applying said flowable material between said semiconductor device and said substrate further comprises placing said semiconductor device and said substrate in a chamber, said chamber having an atmosphere therein having a variable pressure, further comprising: varying the pressure of said atmosphere in said chamber for said flowable material substantially filling a gap between said semiconductor device and said substrate.

Regardless, at column 2, lines 55-68; and column 3, lines 1-10, Banerji discloses a process wherein applying a flowable material 22 between a semiconductor device 10 and a substrate 20 comprises placing the semiconductor device and the substrate in a chamber 32 having an atmosphere therein having a variable pressure, and varying the pressure of the atmosphere in the chamber for the flowable material substantially filling a gap 18 between the semiconductor device and the substrate.

Furthermore, it would have been obvious to combine the process of Banerji with the process of Dery because it would facilitate applying the flowable material 140 between the substrate and the semiconductor device.

Applicant's amendment and remarks filed 3-21-5 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant proposes several arguments predicated on the assumption that Dery discloses only a thermosetting underfill material.

These arguments are respectfully traversed because Dery does not disclose only a thermosetting underfill material, and Dery is not necessarily applied to the rejection for a disclosure of not only a thermosetting material.

The remaining arguments have been adequately addressed previously in the record.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will

expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**For information on the status of this application applicant should check PAIR:**

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.**

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m. The fax phone number for group 2800 is (703) 872-9306.



David E. Graybill  
Primary Examiner  
Art Unit 2822

D.G.  
10-Jun-05